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(56) Documents cited

GB A 2163596	GB A 2035685	GB A 2030023
GB A 2028579	GB 1592500	GB 1532293
GB 1523347	US 4532424	US 4354109
US 3801949		

(58) Field of search
H1K
Selected US specifications from IPC sub-classes
G01J H01C H01L

(54) **Thermal detector array**

(57) A thermal detector array comprises discrete thermal detector elements arranged in a two-dimensional array, each element 1 being supported on one side of a layer 3 of resilient low thermal conductivity material which serves also to space said elements apart from one another, an opposite side of said layer carrying a common electrode structure 5 which is in contact with each element and provides interconnections therebetween by means of high thermal resistance electrically conductive tracks 7, each element 1 having an element electrode 9 which is in contact with an inwardly facing surface of the element, each element electrode 9 being connected by means of a bonding member 13 to an input circuit 15 of a semiconductor substrate 11, such that the said bonding members 13 serve to support the layer 3 with respect to the substrate 11, and each element 1 having a radiation absorber 17 associated therewith.

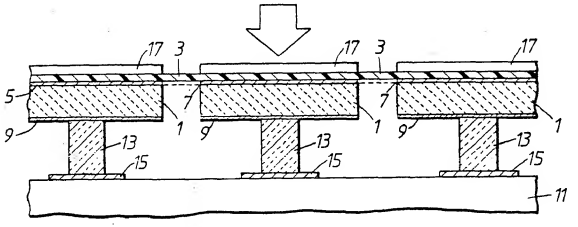

FIG. 1.

The drawing(s) originally filed was (were) informal and the print here reproduced is taken from a later filed formal copy.
The claims were filed later than the filing date within the period prescribed by Rule 25(1) of the Patents Rules 1982.

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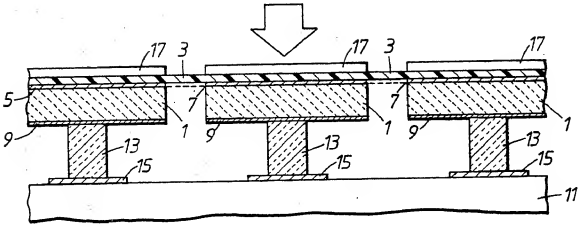

FIG. 1.

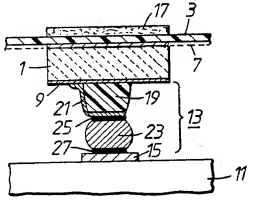

FIG. 2.

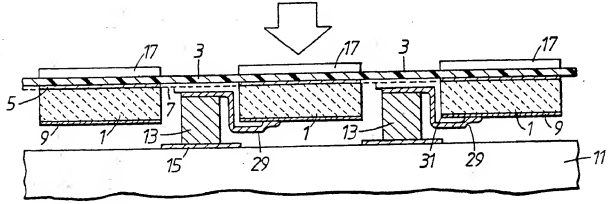

FIG. 3.

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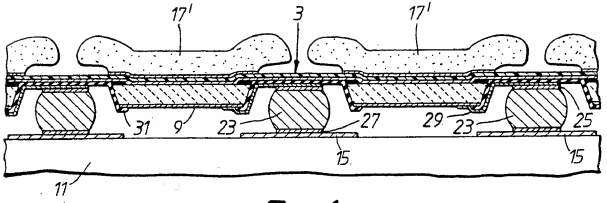

FIG. 4.

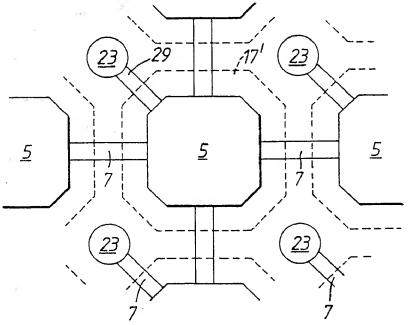

FIG. 5.

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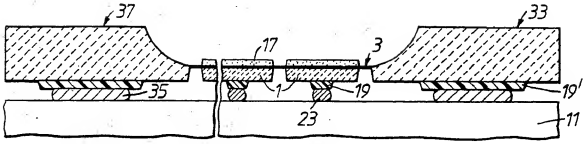

FIG. 6.

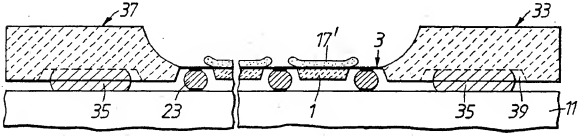

FIG. 7.

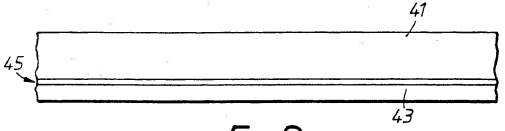

FIG. 8.

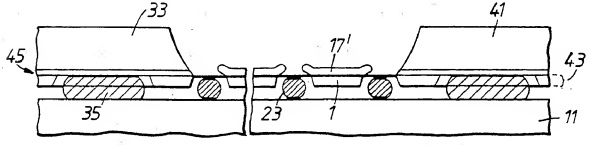

FIG. 9.

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THERMAL DETECTOR ARRAY

TECHNICAL FIELD

The present invention concerns improvements in or relating to thermal detectors and, more particularly, to thermal infra-red detector arrays. In thermal detectors, the energy of the absorbed incident radiation raises the temperature of each detecting element. This increase in temperature causes changes in the temperature dependent properties of the detector which may be monitored to detect the incident radiation. The thermal detectors of specific interest in the present context include pyro-electric detectors and/or dielectric bolometer detectors in the form of a two-dimensional array interfaced to a semiconductor readout device to provide a compact, solid state, uncooled storing array for thermal imaging and related applications.

BACKGROUND ART

There is a growing interest in achieving a thermal detector performance in large two-dimensional arrays at fine pitch (for example arrays of up to and in excess of 100 x 100 elements at pitches at and below 100μm) that approaches the fundamental physical limits for a thermal detector. This performance being assessed, for example, in terms of the signal to noise ratio of the detector array. In order to achieve this performance it is

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necessary first to maximise the signal from the device (the responsivity) by optimising the device structure and by appropriate detector material selection (ie. selecting a material with a high responsivity figure of merit), by optimising the electronic readout scheme and minimising all the sources of noise associated, for example, with the detector material dielectric loss, and noise sources in the electronic readout circuitry. However once these noise sources are sufficiently reduced, then a fundamental physically limiting noise is approached that is determined by the thermal conductance from the structure and the efficiency of radiation collection and absorption in the pixel. This limiting noise figure, termed the thermal fluctuation noise limit, is given by the following expression.

$$\text{Thermal Fluctuation Noise Equivalent Power (N.E.P.)} = \left(\frac{4KT^2G_H}{\eta^2}\right)^{\frac{1}{2}}$$

where G_H is the total thermal conductance from an element in the array, η is the efficiency of radiation collection and absorption in the element pixel area, K is the Boltzmann constant and T is the absolute temperature.

It can be further shown that the electrical contribution to the thermal fluctuation noise equivalent power is proportional to

$$Y_H/\eta$$

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where Y_H is the thermal admittance of an element in the array, one part of which is jwC_H,

where w is the devide operating angular frequency and C_H is the element thermal capacitance. This expression implies that low detector element thicknesses are required, such that wC_H is smaller than or similar to the thermal conductance, the real part of Y_H, in the operating frequency range. In practice total thermal conductance values of less than 0.2 $w.au^{-2}\ K^{-1}$ are required, with radiation collection and absorption efficiencies approaching unity, for element pitches at or below 100μm and element thicknesses of less than 15μm (less than 8μm preferred) in order that the thermal fluctuation noise limit still provides a useful device performance, for operating frequencies in the range 10 to 50Hz. For other frequencies the preferred thickness scales inversely with frequency.

A pyroelectric detector, exhibiting improved Noise Equivalent Power performance, is described in UK Patent Application GB 2,100,058 (1982). As disclosed therein, a thermal detective element is mounted adjacent to an absorber of larger area, and is resiliently supported on one or more flexible films. Electrical connection is provided by conductors that extend laterally on the internal surfaces of the films. Whilst this construction

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may be extended longitudinally in the form of a one-dimensional array, the need for lateral extension as aforesaid, generally precludes implimentation in fine pitch two-dimensional form.

A two-dimensional integrated detector array is described in US Patent Serial No: 4,162,420 (1979). In this device, however, the elements are unreticulated. The detector plane is spaced from, but electrically connected to, silicon readout circuitry by means of a series of metallic rods (10μm square and 25μm length). The use of metallic materials in this form, together with the lack of reticulation, results in a device exhibiting relatively poor thermal isolation and thermal cross-talk between the adjacent elements.

It has thus been a problem, hitherto, providing a fine pitch, large two-dimensional infra-red detector integrated array; an array exhibiting satisfactory thermal isolation and low cross-talk.

DISCLOSURE OF THE INVENTION

The present invention is intended to provided detector structures, and also corresponding methods of processing appropriate, for large two-dimensional thermal detector arrays, in which a high degree of thermal isolation (low G_H) is combined with high radiation collection and absorption efficiency.

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In accordance with this invention there is provided a two dimensional thermal detector integrated array comprising a multiplicity of discrete thermal detector elements arranged in a two dimensional array, each spaced and supported apart by means of a common resilient, support layer-or-web of low thermal conductivity material;

a common electrode structure located upon an internal surface of said layer-or-web, adjacent to and in contact with each element, providing interconnection therebetween by means of high thermal resistance, electrically conductive, tracks;

a multiplicity of element electrodes, one corresponding to each element, in contact with an inwardly facing surface of each respective element;

a semiconductor substrate incorporating a like multiplicity of input circuits;

a multiplicity of individual bonding members, one corresponding to each element, providing support between the substrate and the layer-or-web, and, also providing electrical connection between each element electrode and each respective input circuit; and,

a multiplicity of radiation absorbers, located each adjacent to a respective one of the elements.

The bonding members aforesaid may be of low thermal conductivity and located in position between the

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respective elements and the substrate. Alternatively said bonding members may be located adjacent to the side of respective elements, extending directly between the substrate and the layer-or-web.

Methods of processing for the above are also provided in accord with this invention. Such structures as aforesaid may be produced by processing bulk layers of detector material, or may be produced by thin film techniques. Specific detail will be given in the description that follows hereinafter.

These improved structures and processes are appropriate for dielectric bolometer and pyroelectric detector arrays that employ single crystal or ceramic ferroelectric oxide materials such as: barium strantium titanate; lead-magnesium-noibate; lead scandium tantalate; lead-iron-niobate lead-iron-tungstate; and, lead-zircanate/lead-iron-niobate.

The complete physical separation of the detector elements of the thermal detector material in the array, ensures low thermal conductance and low thermal cross-talk between the elements.

The support layer-or-web is preferably of polymer material. Polymer materials are most suitable for the support layer-or-web, as indeed for any other features that involve a mechanical link or support but that also

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require provision of low thermal conductance. Polymer materials, being generally insulating materials with a complex molecular structure, frequently arranged to provided an amorphous rather than a crystalline solid, offer the lowest ambient temperature thermal conductivity values of all the classes of solids, as seen from the table below:-

Material Class	Thermal Conductivity Range (typical) $W.M^{-1}.K^{-1}$
Metals	10-400
Semi-conductors	1-200
Crystalline inorganic solids	2-200
Amorphous inorganic solids	0.8-2.0
Organic polymers	0.1-0.4

A preferred polymer material class for the support layer-or-web is the polyimide family of high temperature polymers. Examples are to be found amongst those that have hitherto been extensively developed as passivation and inter-layer dielectric coatings for application on silicon integrated circuits. A specific example of a polyimide material that has been successfully demonstrated herein

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is the polyimide so called 'PIQ' manufactured by Hitachi. The use of a polyimide support film material, which is tough and flexible with a high glass transition temperature and good adhesion to metal and oxide surfaces, is entirely compatible with the above cited ferroelectric materials and with flip-chip solder bonding, a technique preferred for the present purpose. Polyimide films are applied by spin coating and cured typically between 300 and 350°C. Coating thicknesses over the range $\sim$ 0.2 to 0.2μm are practicable, submicron coatings being preferred. The difference in thermal expansion coefficients of the polyimide film and the ferroelectric oxide materials that form the detector elements ($\sim$ 50ppm.K^{-1} of $<$ 10 ppm.K^{-1}) places the support film under slight positive tension after cool down from the curing stage. This holds the film taut after reticulation and results in low microphony. Other possible polymer materials for use as support film include polyamides, and polyurathanes (including UV curing types) and polymers deposited from the vapour phase (eg. parylene).

The use of a fully discrete element structure, mounted on a polymer support layer-or-web, which is under slight tension, ensures a very low microphonic response. A degree of piezoelectric activity is inherent in both the pyroelectric and in the dielectric bolometer materials

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under the influence of the applied bias field, and detector designs must be conducted to minimise this undersirable response mode.

The radiation absorber, aforementioned, structure may be formed from a thin resistance metal film with an impedance matched to that of free space ($377\sqrt{\ }10$), that may also serve as the common electrode. Such a film will absorb 50% of the incident broad band radiation. Anti-reflection coatings may be added to increase the efficiency of absorption over a more limited wave band. Again the use of a reflective metal element active electrode layer on the opposite face of the detector element, together with knowledge of the infra-red optical properties of the materials in the structure and control of the thickness of the detector element, may be used to further increase the absorption efficiency in the band of interest. Efficiencies of 0.6 to 0.8 in the 8-14μm infra-red band are attainable for such multi-layer structures. However, preferred absorber layer structure comprises a metallic black, such as a platinum black, which offers an absorption efficiency close to unity in a structure of very low thermal mass.

Whilst the absorbers may be of area equal to that of the respective detector elements, the absorber and detector areas in reticulated detector array structures

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can be varied independently. Indeed the independent nature of these two structures may be exploited to achieve high radiation collection and absorption efficiency, combined with a high degree of detector element thermal isolation.

Preferred electrode materials particularly for interconnection tracks between the elements and to the element bonds, include metals, metal alloys, cermets and amorphous metal alloys that are of high thermal resistivity, show good adhesion to the other materials in the structure and can be patterned to provide narrow tracks. Examples include anodised chromium, and nickel-chromium alloy metallic films, chromium-silica cermet films and nickel-indium amorphous metal films. Such films, required at low thickness (eg. 10 to 30μm) and narrow width (eg. 2 to 10μm), may be deposited by a variety of thermal deposition techiques including filament and electron-beam evaporation, or by sputtering. Sputtering processes, and in particular magnetron sputtering processes, are preferred. An electrode comprising one of the above metals with an overcoat of an inert metal of high electrical conductivity such as gold is generally required for the deposition of metallic blacks such as platinum black. The inert, high conductivity metal may be removed from the element

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interconnection tracks after black deposition to remove the associated thermal shunt. Apertures or "via holes' opened in the polymer support film over the elements are desirable to ensure good thermal contact between the absorber and the detector element. If a thin film, impedance matched, absorber structure is employed, then the polymer support film may also serve as an anti-reflection coating for the absorber.

BRIEF INTRODUCTION OF THE DRAWINGS

In the drawings accompanying this specification:-

Figure 1 is an illustrative cross-section view of a thermal detector integrated array, an embodiment of the present invention;

Figure 2 is a detailed cross-section view of a pixel component of the array of figure 1 preceding, showing in detail the structure of the bonding member thereof;

Figure 3 is an illustrative cross-section view of a thermal detector integrated array, an alternative embodiment of the present invention;

Figures 4 and 5 show in cross-section and plan-view respectively, part of an improved variant of the array shown in the preceding figure;

Figures 6 and 7 are schematic cross-sections of the arrays depicted in the preceding figures, showing constructional and assembly detail for bulk material processing; and,

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Figures 8 and 9 are schematic cross-section of a preform and array corresponding to thin film processing.

DESCRIPTION OF PREFERRED EMBODIMENTS

So that the invention may be better understood, embodiments thereof will now be described, given by way of example only, with particular reference to the accompanying drawings aforesaid.

There is shown in figure 1 a thermal detector integrated array. This is comprised of a large number of thermal detector elements 1, each of which is discrete and is spaced in array position by means of a resilient support layer-or-web 3 of low thermal conductivity material. This latter provides sufficient support and mechanical integrity for the assembly. On an inward facing surface of the layer-or-web 3 there extends a common electrode structure 5 which provides interconnection between elements by means of high thermal resistance electrically conductive links 7. The opposite face of each element 1 bears an individual element electrode 9. The supported element array structure is located over a semiconductor substrate 11, and bonding members 13, which also provide support and electrical connection, are included between each element 1 and the substrate 11. These provide electrical continuity between the element electrodes 9 and corresponding input pads 15

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of interface read-out circuits integrated in the semiconductor substrate 11. Corresponding to each detector element 1, a pad 17 of thermal absorber material is provided on the reverse surface of the layer-or-web 3. Thermal contact between each element 1 and absorber 17 is provided, effective thermal conduction being provided across the support (layer) or through metal filled apertures in the support (web).

As shown in figure 2, each bonding member 13 is of composite structure and is located beneath each element 1. This combines the conflicting requirements of electrical interconnection with thermal isolation. This composite structure may be realised for example, by providing a mesa 19 of a low thermal conductivity material, such as a polymer, immediately beneath the detector 1,and running a thin, high thermal resistance metal track 21 to the top of the mesa 19. The metallised polymer mesa 19 is then bonded and electrically connected to the input pad 15 of the readout substrate 11 by, for example, the provision of a solder bond 23 and surface metallisation 25, 27. This structure may also be employed in an inverted form, that is with the solder bond 23 adjacent to the thermal detector element 1 and the polymer mesa 19 adjacent to the readout substrate 11. However this structure is less favoured as the solder bond 23 now acts as a thermal load

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on the detector element 1 and reduces the responsivity accordingly.

A range of polymer materials may be seleted to form the polymer mesa 19. Polyimide materials are particularly suited for the inverted form of the mesa structure, where the mesa 19 is located on the substrate 11. Polyimide materials are less suited for the original mesa structure because the curing cycle involved can cause some difficulties in the device process sequence. The use of a Novolac photoresist that can be patterned and then flow-baked to form a mesa 19 with a rounded edge profile to facilitate subsequent metallisation is preferred for the structure of figure 2. A radiation (UV, x-ray or electron beam) or chemical (for example an immersion in acidified fomaldehyde solution) stabilisation treatment to cross-link the Novolac resin and to stabilise the mesa dimensions prior to metallisation and the final solder bonding operation, is desirable in this case.

The adoption of a dot bonded structure, where the bonds 13 are located beneath each element 1, means that the element itself can fill a large proportion of the available pixel area. It can be shown that an optimised compromise between pixel fill factor (ie. radiation collection efficiency) and thermal cross-talk between adjacent elements 1 is obtained, for equal absorber 17 and

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element 1 areas, at an element to gap width ratio of 4:1, equivalent to a radiation collection efficiency of 0.64, the use of an extended area platinum black collector (see figure 4) and/or related extended area collector (XAC) structures, can provide a further significant gain in collection efficiency without compromising thermal isolation. A collection and absorption efficiency of approaching 0.9 can be provided by such means, particularly for structures at or below 100μm pitch.

An alternative array structure is shown in figure 3. In this example, thermal isolation of the element 1 from the readout circuit substrate (the dominant heatsink in either structure), and between adjacent elements 1, is achieved simultaneously by means of a band of polymer support webbing 3 around each element 1. The individual elements 1 in this structure are smaller than for the dot bonded structure (figure 1) and the polymer support web 3 correspondingly longer. The bonds 13 that provide the electrical connections from the element electrodes 9 to the readout circuitry 15 are placed upon the web 3, and it is no longer essential to incorporate additional thermal barrier structures (mesas) in the bond 13 as was done for the dot bonded structure. In this structure total thermal conductance is compromised relative to radiation collection efficiency (for the case where the element 1

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and absorber 17 areas are equal) and an optimum element diameter is about 0.6 of the pixel width, giving a pixel fill factor (or radiation collection efficiency) of about 0.35. The total and the lateral thermal conductance values for this polymer pellicle structure are significantly lower than for the dot bonded structure (figure 1) at a given pitch and for practicable structure geometries. This can then provide a superior ultimate device performance, provided the radiation collection efficiency can be increased.

A preferred embodiment of the pellicle mounted two-dimensional thermal detector array structure, incorporates an extended area platinum black collector 17' (PB-XAC), as shown in figure 4. A particular point to note is that this preferred structure includes the trunkation of the element corners (giving octagonal rather than square elements). This increases the length of thin film metallisation track 29 that links each element electrode 9 to each bond connection 13 to the readout circuit 15, providing a further increase in thermal isolation, with minimum loss of absorber area. This thin film track 29 runs from the element electrode 9 over polymer insulation 31 to the point where the bonds 13 are placed. The use of four common electrode connections 7 should also be noted. While two connections per element 1, plus additional

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links at the end of each element row, are sufficient for the complete common connection, some redundancy is useful at the fine track geometries desirable in these fine pitch structures. The use of three or four common connections 7 is therefore desirable. Again flip-chip solder bonding has been adopted as the preferred method for making the bonds 13 between the array and the electronic readout circuit 15. This technique is particularly appropriate to the pellicle mounted structure since the solder bonding process involves no applied mechanical pressure (as required in any solid phase bonding process such as indium bonding), which would be incompatible with bond location on flexible polymer film. The solder bonding process rather relies upon the natural wetting action of molten solder to the wettable metallisation 25, 27 provided on the two components to form the bonds 13. The aspect ratio of the solder bond, with a bond height compatable to the solder wettable pad diameter, allows each thermal detector element 1 to be physically spaced from the readout circuit substrate 11, provided the element thickness is less than the solder bond height. This bond geometry requirement is consistent with the need for very low element thicknesses, as referred to earlier.

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ARRAY FABRICATION

Examples of methods to fabricate thermal detector arrays with the structures described earlier are now considered. These methods, while containing certain novel features, are not necessarily the only methods or sequence of methods by which such arrays may be fabricated. Methods appropriate to detector arrays prepared from bulk ferroelectric materials and from deposited thin ferroelectric films will be described. Particular features include methods for selective thinning and for element reticulation, novel structures to provide mechanical support for the arrays, and methods for hybrid device alignment.

THINNED BULK MATERIAL DEVICES

The structures of two-dimensional thermal detector arrays of the dot-bonded and of the polymer pellicle mounted variety, as fabricated from thinned bulk materials, are illustrated in figures 6 and 7. These figures show the edges of the array structure as well as part of the array area itself. The edges of the device structure comprise a relatively thick, unreticulated 'picture-frame' border 33 around the whole of the detector array. This border provides a sufficiently rigid mechanical, supporting frame for the polymer support or pellicle film 3. It also provides a region of the

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device structure that may be contacted during assembly, and a location for the siting of one or more rows of solder bonds 35 of substantially larger diameter than the solder bonds 23 in the array itself. These layer diameter solder bonds 35 are present to automatically align the hybrid device structure during bonding, in particular to align the array of small diameter array element bonds 23 to the substrate 11.

A possible fabrication sequence for devices, as shown in figures 6 and 7, involves the orientation, cutting, lapping and polishing of the bulk ferroelectric material, either in single crystal or in polycrystalline ceramic form, to provide a parallel sided wafer of the thickness desired for the unreticulated border 33 of the device. The region from which the reticulated array is to be fabricated is then selectively thinned to the final device thickness. Appropriate selective thinning techniques may include various wet and dry etching processes, for example optically enhanced chemical etching or ion beam etching, depending upon the material and its crystal form. Ion beam etching has the advantage of being a relatively universal etching method, and is therefore preferred in many instances. The regions that are not to be thinned are appropriately masked from the etchants using, for example, a metal foil mask or a photoresist layer

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according to the etching procedure.

The various layers required for what will be the incident radiation face 37 of the device are then added into selectively thinned wells. These will commonly include an etch stop layer for the subsequent reticulation operation, the polymer support film or pellicle layer 3, the common electrode layers 5 and the infra-red absorber structure 17. The wafer is then inverted and the element electrodes 9 and reticulation masking layers added. Reticulation is preferably conducted by an anisotropic etching process, such as ion beam etching or reactive ion etching. Masking materials and etch stop layers may be selected appropriately according to the material to be etched, the etching process and the geometry involved. A set of wells 39 may be etched beneath the device support border 33 simultaneously with the reticulation of the element in the array, to later accept the larger diameter alignment solder bonds 35. Etched wells 39 are particularly appropriate for the pellicle mounted structure as can be seen in figure 7. If the solder bonds 23, 35 are defined on the silicon-readout-chip-half of the final hybrid device, then these wells 39 can also aid the mechanical alignment of the components prior to fusing the solder to complete the bonding of the hybrid device. As reticulation

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is completed the etch stop layer serves to protect the underlying polymer support or pellicle film 3. The etch stop layer, having served its purpose may then be removed if desired.

After reticulation is completed, the various layers required for the element connection side of the structure are then added. These may include polymer insulation 31, element electrode 9 and polymer mesa layers 19, element-to-readout interconnection tracks 21 and wettable metallisation pads 25, 27 to accept the solder bonds 23. A corresponding set of wettable metallisation pads 27 are provided on the input pads 15 to the silicon readout circuit. The solder bumps 23 may be defined on either or both components of the hybrid device.

DEPOSITED THIN FILM DEVICES

The ferroelectric materials that form the sensitive elements of the thermal detector array may also be conveniently deposited directly in the form of a thin film at the desired active element thickness. This can avoid potentially costly crystal growth, ceramic fabrication, orientation, cutting, lapping and polishing procedures inherent in the use of bulk materials for these devices. Methods for the thin film deposition of such ferroelectric materials include reactive sputtering from compound targets, metal-organic chemical vapour deposition

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(MOCVD), and in-situ decomposition of deposited metal-organic precursor films (for example films produced by the sol-gel process or by in-situ hydrolysis of spun-on metal-organic complex solutions). Such films can be polycrystalline with various degrees of preferred crystallagraphic orientation, or single crystal in nature depending upon the conditions of deposition and/or decomposition. Particularly important parameters in this regard include the deposition or decomposition temperature, and the nature of the substrate upon which the films are deposited. These processes, for such relatively complex materials as the ferroelectric oxides cited earlier, generally involve deposition or decompositions temperatures in excess of 400°C, particularly if highly crystalline films with preferred orientation or single crystal films are desired. For this reason, direct deposition onto a suitable thermal isolation structure already in place on the readout device is generally difficult. Film deposition, therefore, is preferably made onto a suitable temporary substrate. A substrate 41 with a deposited ferroelectric film 43 and a 'barrier' layer 45 is illustrated in figure 8. The selection of the appropriate refractory substrate material can remove the deposition process temperature constraint mentioned above, and can also open up prospects for controlling film

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structure. Suitable substrate materials may include amorphous materials (eg. fused quartz), and crystalline oxide and other inorganic compound materials. Single crystal substrate materials (eg. spinel, sapphire, magnesium, oxide, cubic zirconia, sodium chloride and lithium fluoride) are of particular interest since they allow the possibility for epitaxial growth of single crystal ferroelectric films, if the lattice parameters or lattice spacings are suitably matched. Single crystal ferroelectric films of the correct orientation can provide a higher material 'figure-of-merit' (for example through a lower dielectric loss than the equivalent polycrystalline film).

The 'barrier' layer 45 shown in figure 8 may be required to avoid chemical interaction of the growing film with the substrate and/or to aid nucleation of the film. The 'barrier' film 45 may itself be deposited onto the substrate 41 so as to provide preferred orientation or as an epitaxial single crystal layer. The preferred orientation or single crystal nature of this 'barrier' film may translate into the ferroelectric film grown thereon. The barrier film 45 may also be used to achieve a gradual transition between the lattice parameter of the substrate 41 to that of the ferroelectric film 43, in the situation where epitaxial growth occurs. An example

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of a barrier layer 45 is metallic platinum, which may be deposited with preferred orientation onto fused quartz, or deposited as an epitaxial film onto single crystal magnesium oxide by sputtering.

Having deposited a ferroelectric thin film 43 of the required thickness onto the substrate 41, this structure may then be processed in a very similar manner to the device structure prepared from the bulk material, as shown in figure 9. The substrate layer 41 is etched away from the active area of the array in a manner appropriate to the substrate material selected, but is retained around the perimeter of the structure to provide the thicker, unreticulated supporting frame 33 for the polymer support or pellicle film 3 that carries the detector array. The barrier layer 45 may be included in the array structure or removed as appropriate. Device processing otherwise follows an entirely similar route to that described earlier and results in a physically similar structure.

Other structural variants that may be derived from the structures described earlier are also included within the scope of this invention. Particular examples include the use of alternative arrangements for concentrating and/or collecting the incident infra-red radiation into the detector elements 1. Thus refractive or reflective optical structures, including miniature, individual

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element immersion optic lenses, and plane facetted or curved reflective funnel structures are included. Such structures may be fabricated for example by the photo-chemical or anisotroptic chemical etching of single crystal silicas, followed by appropriate anit-reflection or metallization coating. Such concentrator structures may again be assembled to, and accurately aligned with, the hybrid device by the use of flip-chip solder bonding.

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CLAIMS:

1. A thermal detector array comprising discrete thermal detector elements arranged in a two-dimensional array, each element being supported on one side of a layer of low thermal conductivity material which serves also to space said elements apart from one another, an opposite side of said layer carrying a common electrode structure which is in contact with each element and provides interconnections there between by means of high thermal resistance, electrically conductive tracks , each element having an element electrode which is in contact with an inwardly facing surface of the element, each element electrode being connected by means of a bonding member to an input circuit of a semiconductor substrate, such that the said bonding members serve to support the layer with respect to the substrate, and each element having a radiation absorbr associated therewith.

2. An array as claimed in claim 1, in which the bonding members are formed of low themal conductivity material.

3. An array as claimed in claim 1 or 2, in which the bonding members are positioned between the respective elements and the substrate.

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4. An array as claimed in Claim 1 or 2, in which the bonding members are located adjacent to the sides of the respective elements, extending directly betwen the substrate and the layer.

5. A thermal detector array substantially as hereinbefore described with reference to any one of the accompanying drawings.

6. A method of manufacturing a thermal detector array substantially as hereinbefore described.

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